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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,926	09/18/2001	Catherine Mallardeau	00-GR1-374	9396

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,926	MALLARDEAU ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7,9-23,33,34 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,9-23,33,34 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Cancellations

1. Applicant's cancellation of Claims 1 – 6, 8, 30 – 32, 35, 36, and 38 in Letter of 13 September 2004 is acknowledged.

Claim Rejections – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 7, 9, 15, 19, 20, 33, 34, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Sung et al. (US 6,1`33,599).

4. Regarding Claims 7 and 34, Sung et al. disclose an integrated circuit having a plurality of transistors, a plurality of passive components (Col. 3, lines 40 – 51), and a level of local metal interconnections (17a,17b) (Figure 9) formed within a first insulating layer (11) that is deposited on top of transistors of the integrated circuit, said integrated circuit comprising:

a first metal terminal (17a) constituting a first stage of contact between one active area (20) and a first level of interconnection (26), having a lower surface that contacts the one active area of the integrated circuit, and having an upper surface that contacts a

second stage of contact between the one active area and the first level of interconnection (26),

a second metal terminal (17b) vertically connecting one active area of the integrated circuit to a passive component (21) that directly contacts the upper surface of the first insulating layer (11), and

a third metal terminal (left side, Figure 9) horizontally connecting two separate active areas (source/drain and gate) of the integrated circuit,

wherein each of the first, second, and third metal terminals consists of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer (11), and

a second metal terminal (17b) has a lower surface that contacts a junction of one of the transistors of the integrated circuit such that the lower surface of the second metal terminal extends over a boundary of the junction of the one transistor.

5. Regarding Claim 9, Sung et al. disclose an integrated circuit wherein the passive component (21) is a capacitor (Col. 6, lines 43 – 44).

6. Regarding Claims 14 and 19, Sung et al. disclose an integrated circuit comprising:

an onboard memory plane of DRAM cells (Col. 2, lines 24 – 26) in a matrix, each of the cells including a control transistor and a storage capacitor (Col. 3, lines 40 – 51),

a plurality of MOS transistors (Figure 9),

a first level of interconnection above the storage capacitors (26),

a first insulating layer (11) separating the MOS transistors and the base of the storage capacitors (21), and

a level of local connections including three metal terminals (17a,17b,17b) each opening onto each side of the first insulating layer, each of the three metal terminals consisting of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer such that the metal terminal passes completely through the thickness of the first insulating layer,

wherein the first metal terminal (17a) forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection (26), has an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and extends from the one active area of the integrated circuit to the second stage of contact,

the second metal terminal (17b) vertically connects one active area of the integrated circuit with one plate of the one storage capacitor extending over a boundary of an upper sur-Face of the second metal terminal so that a portion of the lower surface of the one plate rests on the upper surface of the second metal terminal and the remainder of the lower surface of the one plate rests on the upper surface of the first insulating layer, and

a third metal terminal (left side, Figure 9) horizontally connecting two separate active areas (source/drain and gate) of the integrated circuit.

7. Regarding Claims 15 and 20, Sung et al. disclose an integrated circuit wherein the second metal terminal (17b) has a lower surface that contacts a junction of the one active area such that the lower surface of the second metal terminal extends over à boundary of the junction.

8. Regarding Claim 33, Sung et al. disclose that the first insulating layer (11) is a single layer and the only insulating layer provided between the transistors and the base of the passive component.

9. Regarding Claim 37, Sung et al. disclose an integrated circuit wherein the second metal terminal (17b) (Figure 9) has an upper surface that contacts a base of the passive component (21) and a lower surface of the base of the passive component rests on the upper surface of the second metal terminal and the remainder of the lower surface of the base of the passive component rests on an upper surface of the first insulating layer.

Claim Rejections – 35 U.S.C. 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al., as applied to Claims 7, 9, 14, 15, 19, 20, 33, 34, and 37, and further in view of Maeda (US 6,358,820 B1).

12. Regarding Claim 10, Sung et al. do not disclose that the passive component is an inductor. However, Maeda discloses (Col. 7, lines 3 – 17) an inductor (20) (Figure 1) within an insulating film (silicon oxide) formed on a first insulating structure (Figure 15)

and electrically connected to a junction through interconnects. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sung et al. and Maeda to provide a means of incorporating an inductor on an insulating film above an active region with reduced parasitic capacitance in an integrated circuit.

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al., as applied to Claims 7, 9, 14, 15, 19, 20, 33, 34, and 37.

14. Regarding Claim 13, Sung et al. do not explicitly disclose that the thickness of the second insulating layer is 2 micrometers. However, varying the thickness of insulating layers to determine the optimal value in a device structure is routine in the art. It would therefore, have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the thickness of the second insulating layer within the range as claimed to attain a working device.

15. Claims 11, 17, 18, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al., as applied to Claims 7, 9, 14, 15, 19, 20, 33, 34, and 37, and further in view of Deboer et al. (US 6,677,636 B2).

16. Regarding Claim 11, Sung et al. disclose that the thickness of the first insulating region is greater than 0.3 um (3000 Angstroms) (Col. 5, lines 4 – 6) and the top upper surface of the first insulating layer is plane (Col. 5, lines 6 – 9). Sung et al. do not disclose that the first, second, and third metal terminals are made of tungsten. Deboer et al. disclose the presence of contact plugs (39) (Figure made of tungsten (Col. 4, lines 56 – 64). It would have been obvious to one

of ordinary skill in the art at the time of the invention to combine Deboer et al. with Sung et al. to obtain plugs with good step coverage (Deboer et al., Col. 4, lines 62 – 63).

17. Regarding Claims 17 and 22, Sung et al. do not disclose the presence of a third insulating layer with a contact opening passing through the second and third layers to the upper surface of the first metal terminal. Deboer et al. disclose the presence of a third insulating layer (64) (Figure 8) above the second insulating layer (44) and opening onto the upper surface of the first metal terminal (41). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Deboer et al. with Sung et al. to obtain a device with increased inter-connection capability.

18. Regarding Claims 18 and 23, Sung et al. do not disclose that the first, second, and third metal terminals are made of tungsten. Deboer et al. disclose the presence of contact plugs (39) (Figure 8) made of tungsten (Col. 4, lines 56 – 64). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Deboer et al. with Sung et al. to obtain plugs with good step coverage (Deboer et al., Col. 4, lines 62 – 63).

Claim Objections

19. Claims 12, 16, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A review of the prior art shows that in the claims of the instant application, an integrated circuit having *"a cavity passing through the entire thickness of the*

second insulating layer and opening onto the upper surface of the second metal terminal, wherein the one plate of the one storage capacitor carpets the bottom and inside flanks of the cavity," wherein, *"a portion of the lower surface of the one plate rests on the upper surface of the second metal terminal and the remainder rests on the upper surface of the first insulating layer,"* is not taught or suggested in the art.

Response to Arguments

20. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusions

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30 to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
March 12, 2004

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